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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/615,705	07/13/00	HORIGUCHI	Y 060098

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EXAMINER	
NADAV,O	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/615,705	Horiguchi
Examiner	**Art Unit**
ORI NADAV	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 3, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above, claim(s) *2, 4-7, 9, 11, and 14-19* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3, 8, 10, 12, and 13* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 7/3/2001 have been approved by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 8, 10, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3, 8, 10, 12 and 13 depend on non-elected claims, thus rendering them indefinite.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 8, 10, 12 and 13, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al. (4,456,939) in view of Miller (5,255,146).

Ozaki et al. teach in figure 2 a semiconductor device comprising a MOS capacitor 106 connected between a power source wire 107 and a ground potential wire, a power source terminal 103 to which voltage is applied, a ground terminal to which the ground potential wire is connected, and an ESD being a MOSFET connected in parallel with the capacitor, the drain of which is connected to the power source wire and the source and gate of which are connected to the ground potential wire.

Although Ozaki et al. do not state a MOS capacitor, MIS capacitor 106 includes a MOS capacitor, because it is conventional to form a gate dielectric comprising oxide, of which official notice may be taken.

Ozaki et al. do not teach a wire resistance of the ground potential between the ESD element connection point and the ground terminal being larger than that between the ESD element connection point and the MOS capacitor's connection point.

A wire resistance is directly proportional to the length of the wire. Therefore, Ozaki et al. do not teach the layout design of the device, wherein the ground terminal being further away from the ESD element connection point than the distance between the element connection point and the MOS capacitor's connection point. In other words,

Ozaki et al. do not teach the ESD protection circuit being located further from the ground pad.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a layout wherein the ground terminal being further away from the ESD element connection point than the distance between the element connection point and the MOS capacitor's connection point in Ozaki et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization. Note that computer-aided design of integrated circuits is conventionally used nowadays to design semiconductor layouts, of which official notice may be taken.

In the alternative, Miller teaches in figure 2 ESD protection circuits 14 being located further from the ground pad 12a, such that the wire resistance of the ground potential between the ESD circuit connection point and the ground terminal is larger than that between the ESD elements within the ESD circuit to the ground connection point.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the circuit layout of Miller in Ozaki et al.'s device, since it is conventional to connect the ESD protection circuit to a spaced apart ground pad, of which judicial notice may be taken.

Regarding claim 3, Ozaki et al. teach no other diffusion layer except the ESD element is connected on the ground potential wire between the ground terminal and the connection point on the ground potential wire with one end of the MOS capacitor.

Regarding claim 10, although Ozaki et al. do not explicitly disclose the ESD element clamps a voltage applied to both terminals at a clamp voltage which is lower than the dielectric breakdown voltage of the MOS capacitor, this feature is inherent in Ozaki et al.'s device, because Ozaki et al.'s structure is identical to the claimed structure.

Response to Arguments

6. Applicant argues on page 7 that the limitations of claim 16 are recited in the text of the embodiment of figure 1, because the written description of the first embodiment teaches that the device of figure 1 can apply to a thyristor.

Although the written description of the first embodiment teaches that the device of figure 1 can apply to a thyristor, the claimed limitations of "a thyristor constituted by forming on a substrate having....closely face each other", are not recited in the written description of the first embodiment, but rather in the description of the second embodiment on pages 21-22. Therefore, claim 16 is drawn to non-elected embodiment

7. Applicant requests the examiner to consider claim 18, because claim 18 should have been elected.

Claim 18 was withdrawn from consideration upon applicant's election in paper 5. Examination of claim 18 would be considered when continued prosecution or continued examination application is filed.

8. Applicant argues on page 8 that the examiner did not cite any references regarding the official notice of positioning an ESD element with respect to an MOS capacitor, such that the wire resistance of the ground potential between the ESD element connection point and the ground terminal is larger than that between the ESD element connection point and the MOS capacitor's connection point.

The examiner did not take the official notice that positioning an ESD element with respect to an MOS capacitor, such that the wire resistance of the ground potential between the ESD element connection point and the ground terminal is larger than that between the ESD element connection point and the MOS capacitor's connection point, is well known in the art. The examiner took the official notice that it well known to use computers in the design of semiconductor layout. Note Cohn is cited to support the well known position (column 1, lines 11-19).

9. Applicant argues on pages 8 and 9 that the examiner ignores the limitation of a MOS capacitor being in parallel with an ESD element between a power source wire and a ground potential wire.

The examiner does not ignore the limitation of a MOS capacitor being in parallel with an ESD element between a power source wire and a ground potential wire. Ozaki et al. teach in figure 2 a MIS capacitor 106 being in parallel with an ESD element 108 between a power source wire 107 and a ground potential wire Vss, as claimed.

10. Applicant argues on page 9 that the circuit of figure 2 of Ozaki et al. is identical to the circuit of figure 17 f the present application.

The circuit of figure 2 of Ozaki et al. is not identical to the circuit of figure 17 f the present application for at least the following reason. The circuit of figure 2 of Ozaki et al. includes a resistor 104 between the ESD element and the input terminal 103, whereas the circuit of figure 17 f the present application includes a resistor R between the ground terminal and MOS transistor 304.

11. Applicant argues on page 9 that the MIS capacitor of Ozaki et al. is not connected between a power source wire and a ground potential wire.

The MIS capacitor of Ozaki et al. is not connected between a power source wire 107 and a ground potential wire Vss. Node 107 must be connected to a power source wire, because the device would not function without a power source wire.

12. Applicant argues on page 9 that Miller does not teach the resistive relationship as recited in claim 1.

Miller is cited to teach an artisan that ESD protection circuits can be located further from the ground pad. The correlation between (1) the distance between the ESD protection circuit and the ground pad, and (2) the wire resistance was addressed in section 5 of the office action.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference A is cited as being related to using computers in the design of semiconductor layout

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Sara W Crane

Sara Crane
Primary Examiner

Ori Nadav

August 14, 2001